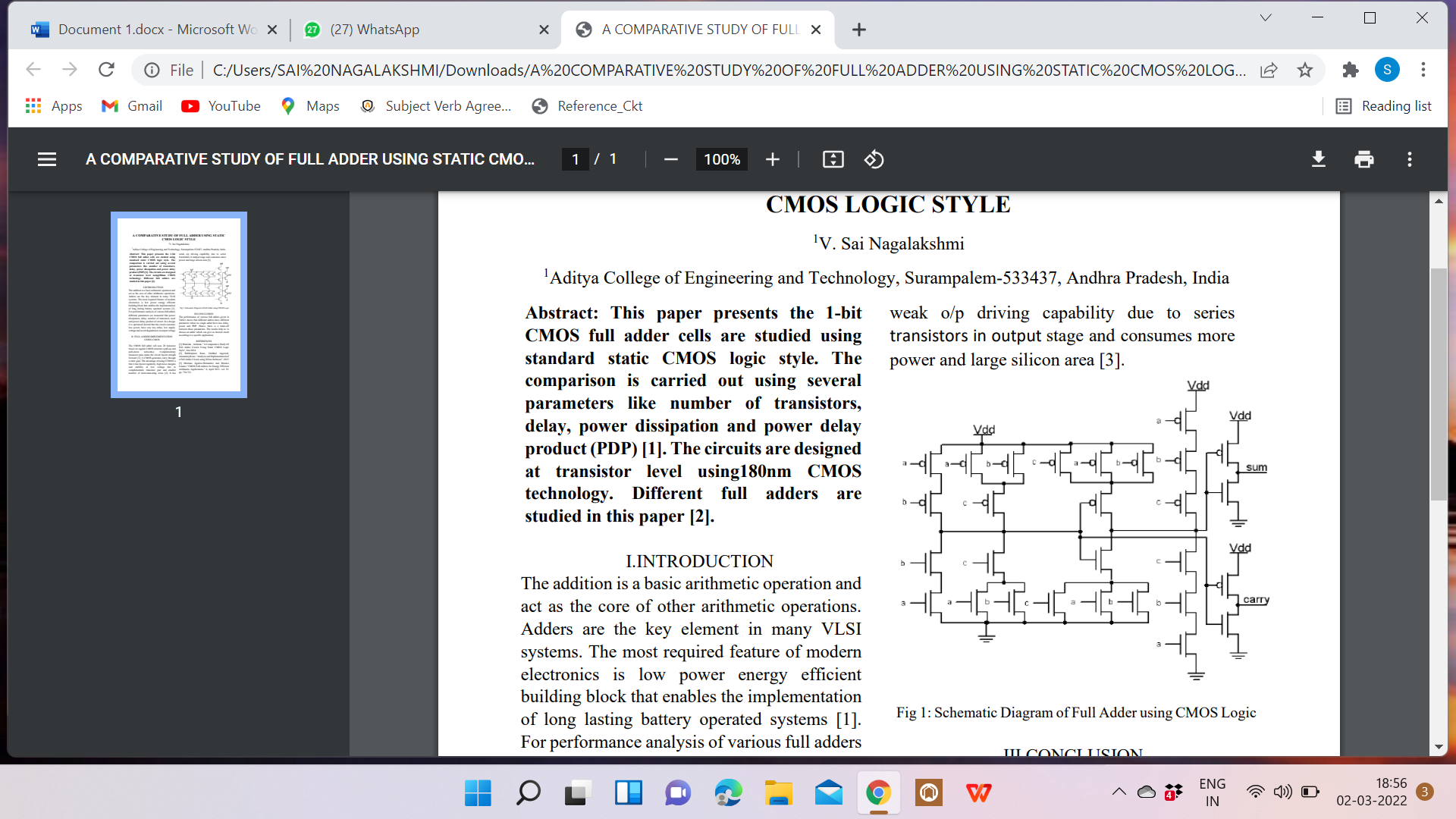
**Full adder using 28nm CMOS technology**

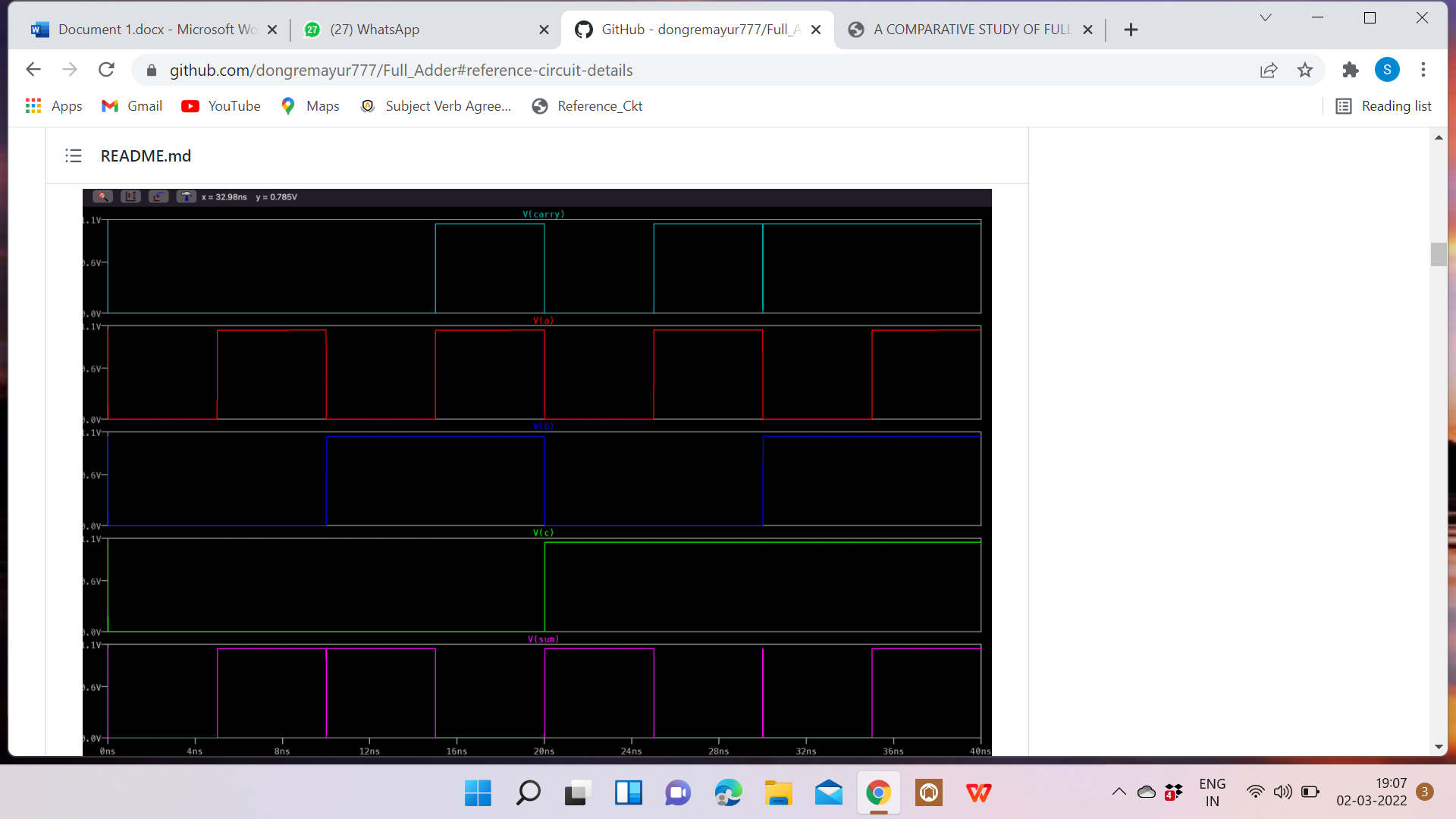
**Abstract**: This paper presents the 1-bit CMOS full adder cells are studied using standard static CMOS logic style. The comparison is carried out using several parameters like number of transistors, delay, power dissipation and power delay product (PDP) [1]. The circuits are designed at transistor level using180nm CMOS technology. Different full adders are studied in this paper.

**Reference circuit details**: Conventional CMOS Full Adder is the most basic full adder implementation techniques. Conventional CMOS Full Adder consists of 28 transistors. A, B and Cin are the inputs and Sum & Cout are the outputs. Static logic provides robustness against noise effects, so automatically provides a reliable operation. Pseudo NMOS pass-transistor logic and reduce the number of transistors required to implement a given logic function but these suffer from static power dissipation. On the other hand, dynamic logic requires less silicon area for implementation of complex function but charge leakage and charge refreshing are required which reduces the frequency of operation. This circuit uses both NMOS and PMOS transistors. In Conventional CMOS Full Adder, there are many leakage paths which lead to more sub threshold leakage.

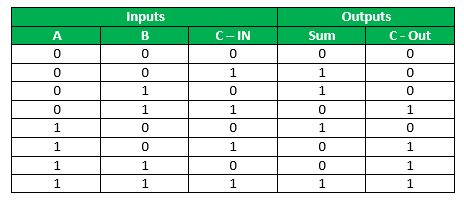
**Reference circuit diagram**:



**Reference circuit waveform**:



**Desirable Truth Table:**



**Tools Used**:

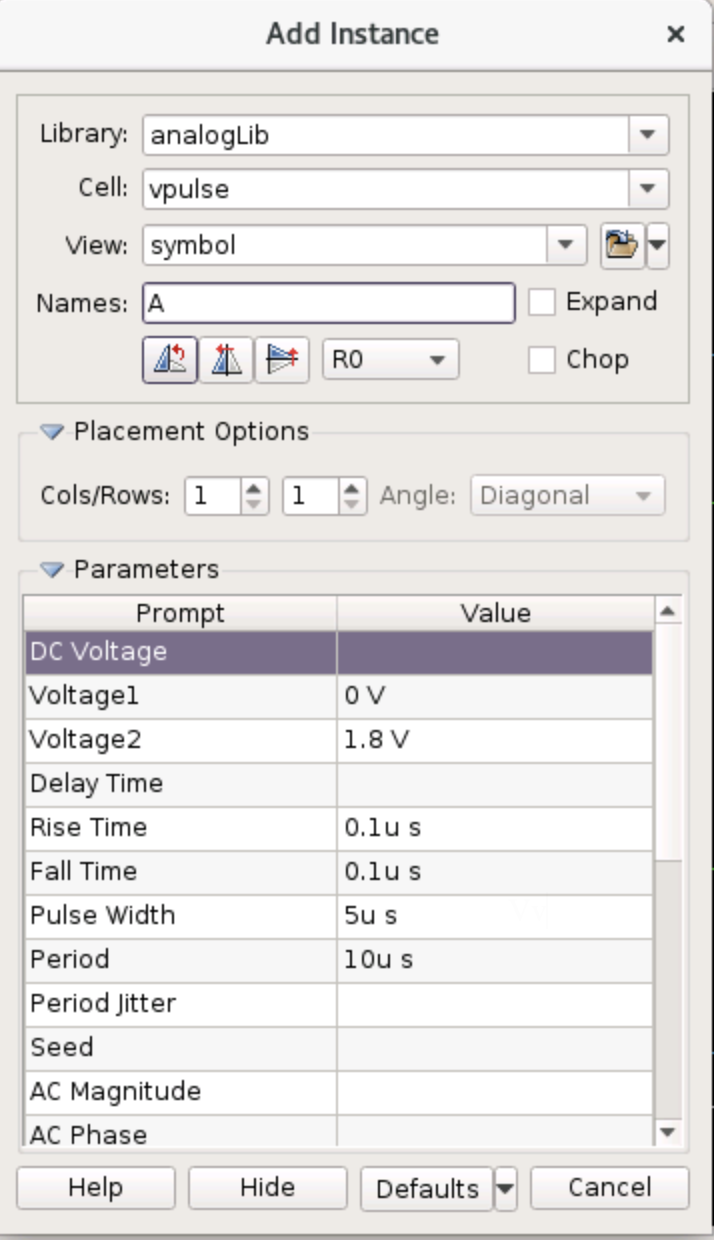
Synopsys Custom Compiler: The Synopsys Custom Compiler™ design environment is a modern solution for full-custom analog, custom digital, and mixed-signal IC design. As the heart of the Synopsys Custom Design Platform, Custom Compiler provides design entry, simulation management and analysis, and custom layout editing features. This tool was used to design the circuit on a transistor level.



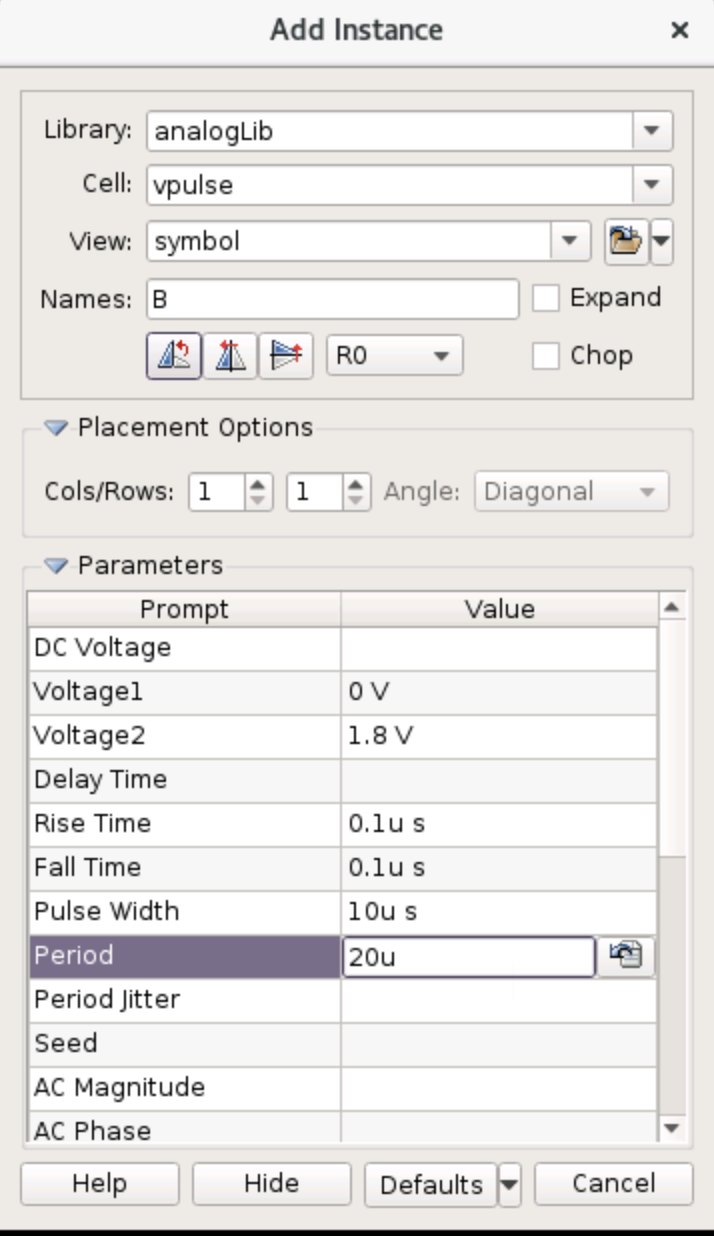
**Synopsys Primewave**: PrimeWave™ Design Environment is a comprehensive and flexible environment for simulation setup and analysis of analog, RF, mixed-signal design, custom-digital and memory designs within the Synopsys Custom Design Platform. This tool helped in various types of simulations of the above designed circuit.

• **Synopsys 28nm PDK:** The Synopsys 28nm Process Design Kit (PDK) was used in creation and simulation of the above designed circuit.

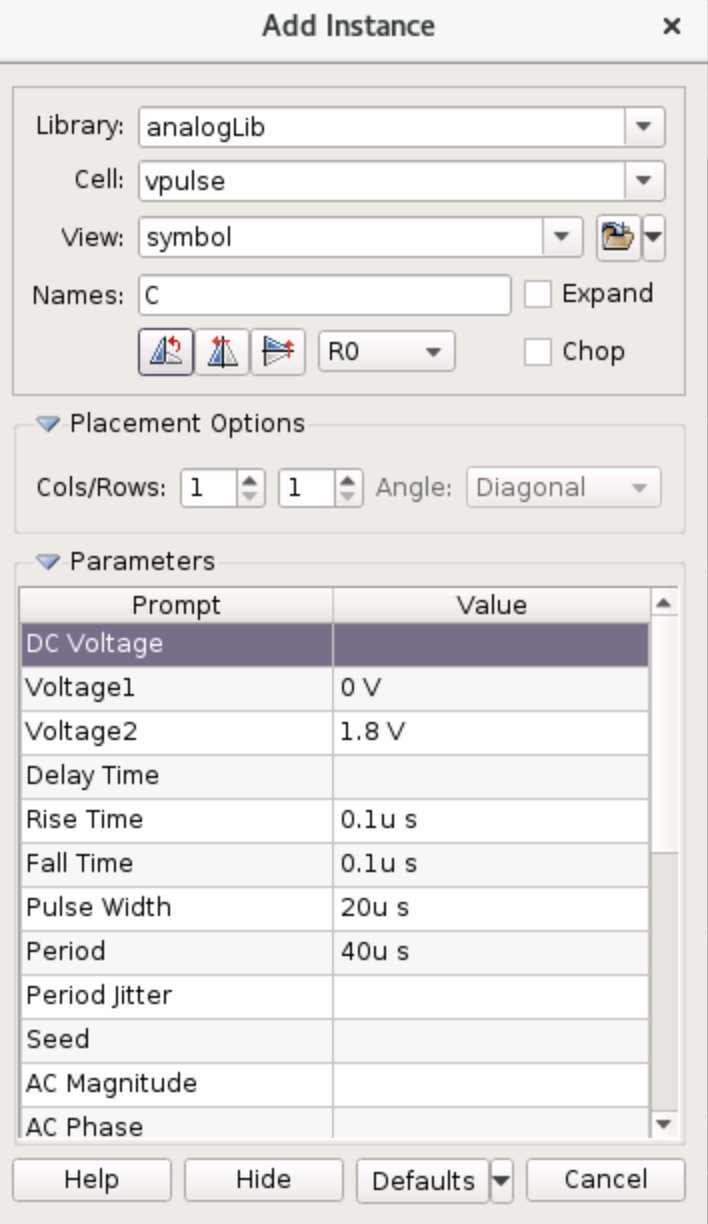
**Parameters set for voltage source for input A:**



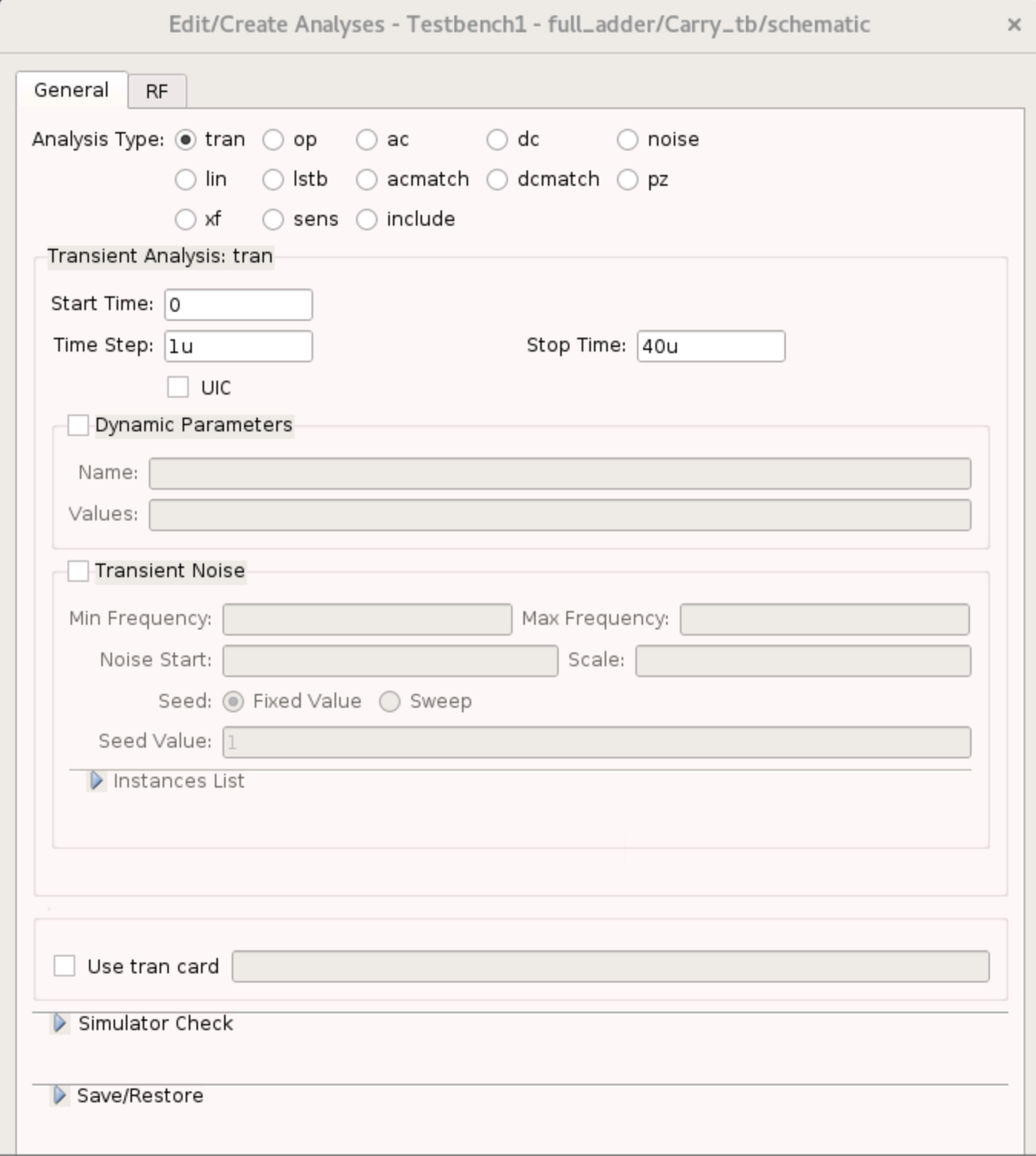
**Parameters set for voltage source for input B**:



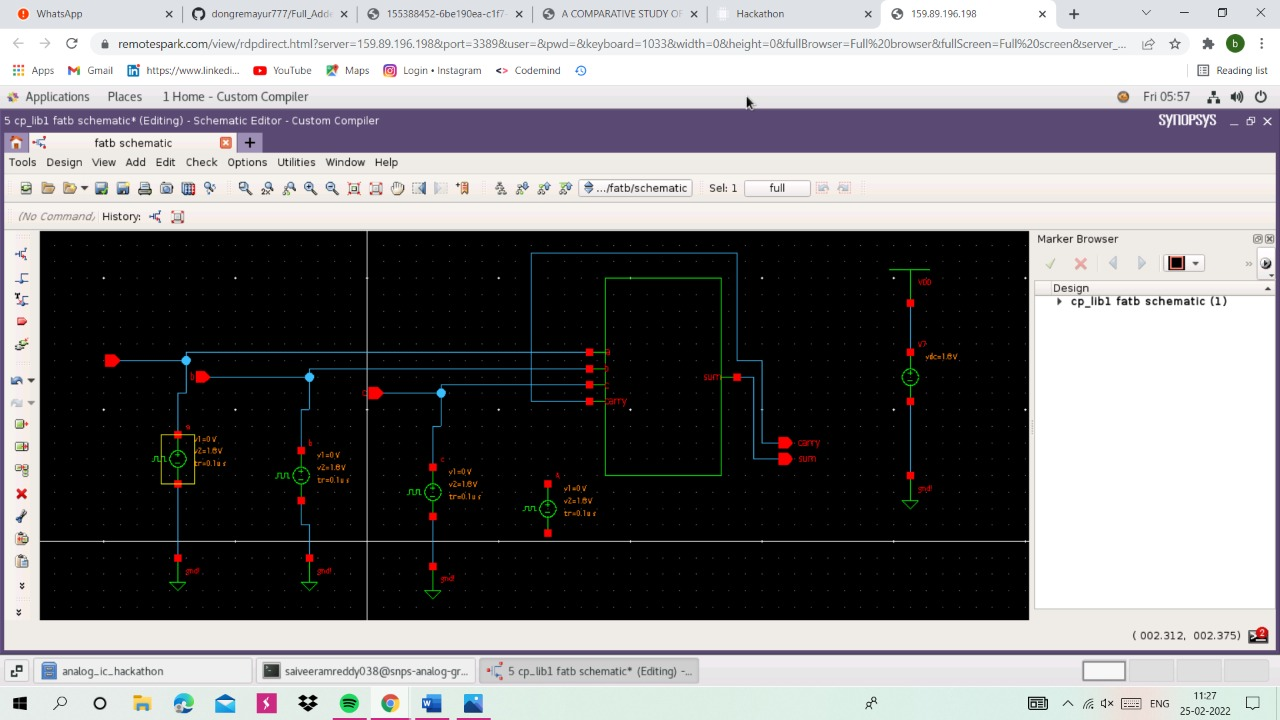
**Parameters set for voltage source for input C**:



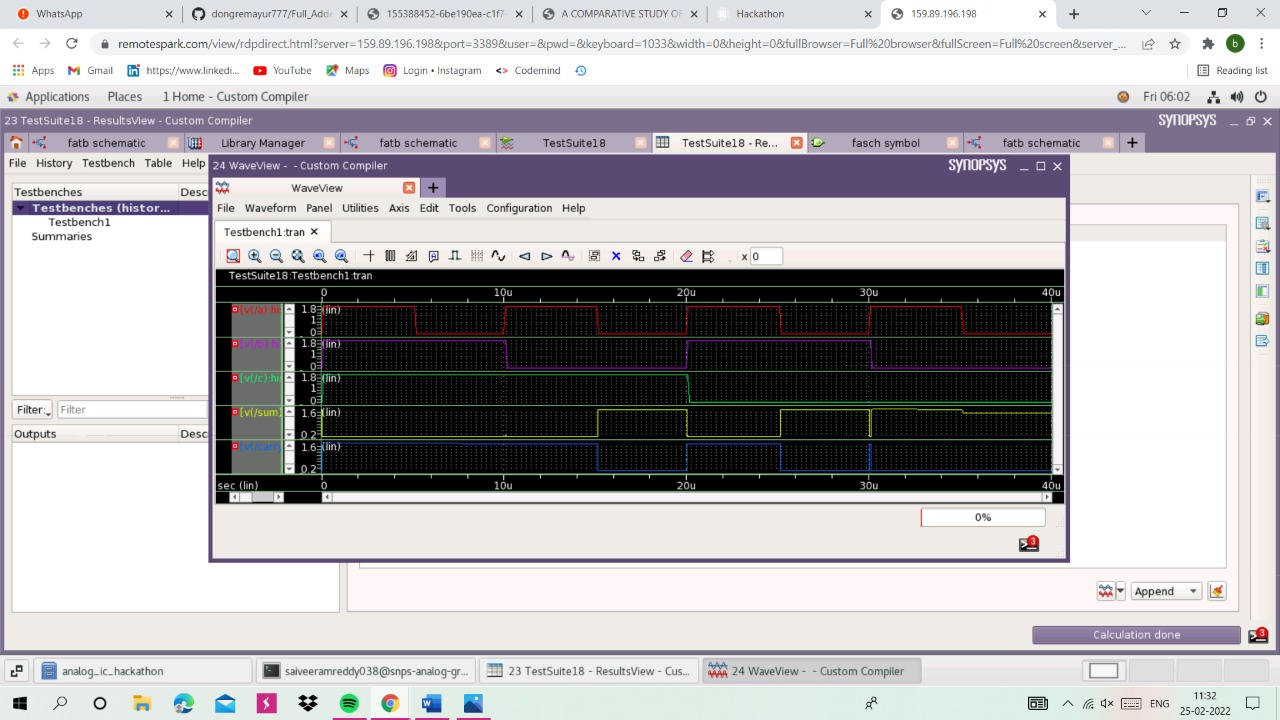
**Transient Settings:**



**Schematic of Full Adder**:



**Output Wavform:**



**Netlist:**

\* Generated for: PrimeSim  
\* Design library name: full\_adder  
\* Design cell name: Carry\_tb  
\* Design view name: schematic  
.lib 'saed32nm.lib' TT  
  
\*Custom Compiler Version S-2021.09  
\*Wed Feb 23 18:37:06 2022  
  
.global gnd!  
\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*  
\* Library : full\_adder  
\* Cell : Carry\_Block  
\* View : schematic  
\* View Search List : hspice hspiceD schematic spice veriloga  
\* View Stop List : hspice hspiceD  
\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*  
.subckt carry\_block a b c gnd\_1 vdd carry  
xm11 carry carry\_bar gnd\_1 gnd\_1 n105 w=0.1u l=0.03u nf=1 m=1  
xm8 net30 a gnd\_1 gnd\_1 n105 w=0.1u l=0.03u nf=1 m=1  
xm7 carry\_bar b net30 gnd\_1 n105 w=0.1u l=0.03u nf=1 m=1  
xm2 net9 b gnd\_1 gnd\_1 n105 w=0.1u l=0.03u nf=1 m=1  
xm1 net9 a gnd\_1 gnd\_1 n105 w=0.1u l=0.03u nf=1 m=1  
xm31 carry\_bar c net9 gnd\_1 n105 w=0.1u l=0.03u nf=1 m=1  
xm12 carry carry\_bar vdd vdd p105 w=0.1u l=0.03u nf=1 m=1  
xm10 net34 a vdd vdd p105 w=0.1u l=0.03u nf=1 m=1  
xm9 carry\_bar b net34 vdd p105 w=0.1u l=0.03u nf=1 m=1  
xm5 net23 b vdd vdd p105 w=0.1u l=0.03u nf=1 m=1  
xm4 net23 a vdd vdd p105 w=0.1u l=0.03u nf=1 m=1  
xm3 carry\_bar c net23 vdd p105 w=0.1u l=0.03u nf=1 m=1  
.ends carry\_block  
  
\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*  
\* Library : full\_adder  
\* Cell : Inverter  
\* View : schematic  
\* View Search List : hspice hspiceD schematic spice veriloga  
\* View Stop List : hspice hspiceD  
\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*  
.subckt inverter gnd\_1 input not vdd  
xm0 not input vdd vdd p105 w=0.1u l=0.03u nf=1 m=1  
xm1 not input gnd\_1 gnd\_1 n105 w=0.1u l=0.03u nf=1 m=1  
.ends inverter  
  
\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*  
\* Library : full\_adder  
\* Cell : Sum\_Block  
\* View : schematic  
\* View Search List : hspice hspiceD schematic spice veriloga  
\* View Stop List : hspice hspiceD  
\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*  
.subckt sum\_block a b c carry\_bar gnd\_1 sum\_bar vdd  
xm29 sum\_bar c net174 vdd p105 w=0.1u l=0.03u nf=1 m=1  
xm30 net174 b net178 vdd p105 w=0.1u l=0.03u nf=1 m=1  
xm31 net178 a net111 vdd p105 w=0.1u l=0.03u nf=1 m=1  
xm18 net111 c vdd vdd p105 w=0.1u l=0.03u nf=1 m=1  
xm19 sum\_bar carry\_bar net111 vdd p105 w=0.1u l=0.03u nf=1 m=1  
xm20 net111 a vdd vdd p105 w=0.1u l=0.03u nf=1 m=1  
xm21 net111 b vdd vdd p105 w=0.1u l=0.03u nf=1 m=1  
xm26 sum\_bar c net160 gnd\_1 n105 w=0.1u l=0.03u nf=1 m=1  
xm28 net164 b gnd\_1 gnd\_1 n105 w=0.1u l=0.03u nf=1 m=1  
xm27 net160 a net164 gnd\_1 n105 w=0.1u l=0.03u nf=1 m=1  
xm23 net150 a gnd\_1 gnd\_1 n105 w=0.1u l=0.03u nf=1 m=1  
xm22 sum\_bar carry\_bar net150 gnd\_1 n105 w=0.1u l=0.03u nf=1 m=1  
xm24 net150 b gnd\_1 gnd\_1 n105 w=0.1u l=0.03u nf=1 m=1  
xm25 net150 c gnd\_1 gnd\_1 n105 w=0.1u l=0.03u nf=1 m=1  
.ends sum\_block  
  
\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*  
\* Library : full\_adder  
\* Cell : Carry\_tb  
\* View : schematic  
\* View Search List : hspice hspiceD schematic spice veriloga  
\* View Stop List : hspice hspiceD  
\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*  
xi24 a b c gnd! net55 carry carry\_block  
v1 net55 gnd! dc='1.8V'  
v22 c gnd! dc=0 pulse ( 0 1.8 0 0.1u 0.1u 20u 40u )  
v21 b gnd! dc=0 pulse ( 0 1.8 0 0.1u 0.1u 10u 20u )  
v20 a gnd! dc=0 pulse ( 0 1.8 0 0.1u 0.1u 5u 10u )  
c2 carry gnd! c=1p  
c19 sum gnd! c=1p  
xi23 gnd! net50 sum net55 inverter  
xi9 gnd! carry net33 net55 inverter  
xi15 a b c net33 gnd! net50 net55 sum\_block  
  
.tran '1u' '40u' name=tran  
  
.option primesim\_remove\_probe\_prefix = 0  
.probe v(\*) i(\*) level=1  
.probe tran v(a) v(b) v(c) v(carry) v(sum)  
  
.temp 25  
  
  
  
.option primesim\_output=wdf  
  
  
.option parhier = LOCAL  
  
  
  
.end

## **Conclusion:**

Thus, the addition for a single-bit is achieved using 28T full adder.

## **Acknowledgement:**

1. Kunal Ghosh, Co-founder, VSD Corp. Pvt. Ltd. - [kunalpghosh@gmail.com](mailto:kunalpghosh@gmail.com)
2. Chinmay panda, IIT Hyderabad
3. Sameer Durgoji, NIT Karnataka
4. [**Synopsys Team/Company**](https://www.synopsys.com/)
5. [**https://www.iith.ac.in/events/2022/02/15/Cloud-Based-Analog-IC-Design-Hackathon/**](https://www.iith.ac.in/events/2022/02/15/Cloud-Based-Analog-IC-Design-Hackathon/)

## **References:**

[1] Manisha , Archana; “A Comparative Study Of Full Adder Circuit Using Static CMOS Logic Style”, Jun-2014.

[2] Bobbinpreet Kaur, Girdhari Agarwal, Amandeep Kaur, “Analysis and Implementation of a Full Adder Circuit using Xilinx Software”, 2015

[3] Mariano Aguirre-Hernandez and Monico Linares “CMOS Full-Adders for Energy Efficient Arithmetic Applications,” 4, April 2011, vol. 19, pp. 718-721.